

A V-Band GaAs MMIC Chip Set on a Highly Reliable WSi/Au Refractory Gate Process

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Abstract

A compact V-band GaAs MMIC chip set consisting of 1) a single highly integrated receiver MMIC with 6.5dB N.F. and 2dB conversion gain using a subharmonically pumped mixer and 2) a transmitter MMIC having a state-of-the-art 30-60GHz doubler with 14.3dB maximum conversion gain, 17.7dBm output power and broadband RF characteristics has been successfully implemented with a refractory WSi/Au gate for high reliability. The HJFETs of these MMICs exhibited an MTTF of 4E7 hours at a channel temperature (T_{ch}) of 130°C. This result demonstrates high potential of our MMIC technology and to enable highly reliable and highly integrated V- and W-band systems.

Introduction

There have been growing demands recently to support short-range systems such as wireless LANs and automobile collision avoidance radars [1]. For these systems, highly reliable, low-cost and reproducible MMICs are required in millimeter-wave frequencies. Several MMICs having AlGaAs /InGaAs pseudomorphic HJFETs have been reported with good performance in the millimeter-wave frequencies [2][3][4]. For simplification of millimeter wave systems, it is essential to avoid use of a high frequency local signal by using a subharmonic mixer and a multiplier. W-band subharmonic mixers which exhibit good RF performance have been developed [5][6]. MMIC doublers for a transmitter have been widely developed. The purpose of this work is to implement a highly reliable and compact V-band chip set. The developed set consists of a high power and high conversion gain transmitter MMIC with a doubler and a receiver MMIC of good RF performance with subharmonic mixer. The transmitter/receiver system is simplified by dispensing of both a power amplifier and a V-band oscillator. This is the first time that a single highly integrated receiver chip with a subharmonic mixer, an LNA for improving conversion gain and noise figure (N.F.) and a local amplifier has been developed. The transmitter MMIC has the state-of-the-art characteristics. Furthermore, the area of developed MMICs is less than half that of multifunctional MMICs, to the best of our knowledge.

MMIC process and their reliability

High reliability millimeter-wave MMICs having 0.18 μ m T-shaped (WSi/Au) gate hetero-junction HJFETs were successfully developed. The HJFETs were fabricated on an MOCVD-grown epitaxial wafer with an n/n AlGaAs top layer. A 0.18 μ m gate was formed (Fig.1) with an optimized, highly reproducible inner side-wall process such that 3σ of the gate length is less than 0.03 μ m. The HJFETs have a double-recessed structure which was optimized for both reliability and RF performance. To improve homogeneity of HJFET parameters, selective dry

etching was employed in the first-recess formation. The HJFETs show an F_{max} of 200GHz, a BV_{gd} of 12V and an I_{max} of 550mA/mm. The mean time to failure (MTTF) of HJFETs was estimated to be greater than 4×10^7 hours (assuming 1.3eV of activation energy) at 130°C junction temperature under typical bias conditions and greater than 10^8 (assuming 1.6eV) hours at 130°C under high temperature storage test conditions.

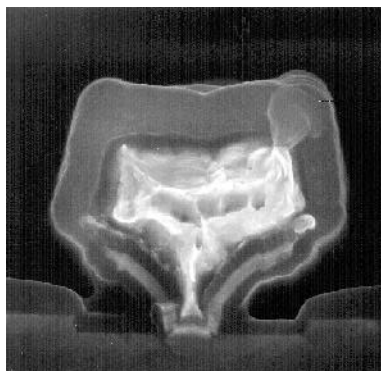


Fig.1 Cross sectional SEM view of the gate

Circuit design

In order to design MMICs, the linear and non-linear parameters of HJFETs and Schottky diode parameters for the subharmonic mixer were extracted from S parameters and DC-IV characteristics. Some empirical passive element models are not accurate enough in designing impedance matching circuits at millimeter-wave frequencies. Among them, the small sized capacitor model is especially inadequate enough because of fringing effects. In order to improve the accuracy of the matching circuit, MIM capacitors (~ 0.08 pF) were measured and remodeled (Fig.2).

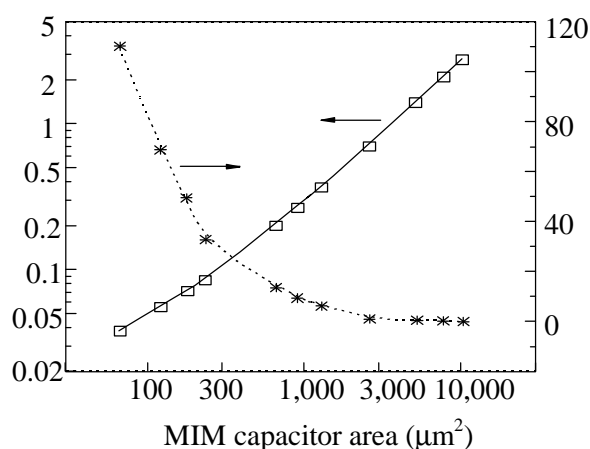


Fig.2 MIM capacitance. *Fringing effect contributes to 80% of the total capacitance associated with a 100 μm^2 MIM capacitor area*

These capacitors were used to obtain a broadband frequency response for an inter-stage conjugate matching circuit. For the remaining passive elements, a quasi-3 dimensional electromagnetic (EM) analysis was employed. The developed MMICs are optimized for small size. It is effective for chip size reduction to diminish the size of impedance matching circuits while maintaining conjugate matching of the inter-stage circuit of HJFETs and function-blocks (i.e. doubler - amplifier). This was achieved by a matching circuit which consists of only two

elements : very small series capacitance and a short or a open stub. Considering the size limitations of a V-band MMIC package and a chip-assembly, the vertical length of MMIC was optimized at less than 0.9mm. Moreover, input and output matching circuits of all V-band MMICs were designed taking into account an inductance of a bonding wire at the chip-assembly.

V-band receiver chip

The receiver chip is a highly integrated MMIC which has an LNA(low noise amplifier), a subharmonically pumped mixer and a local signal amplifier. Fig.3 shows the block diagram of this receiver chip.

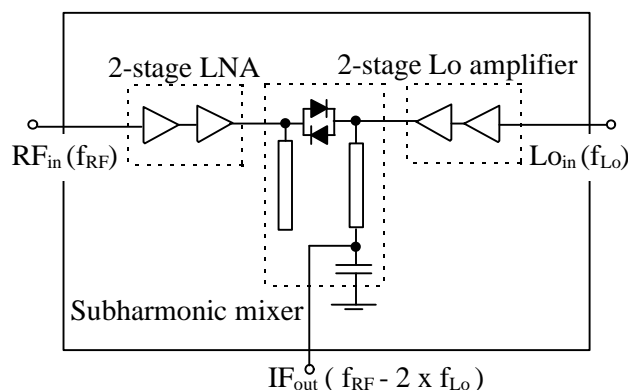


Fig.3 Block diagram of Receiver MMIC

The LNA is a 2-stage reactive matched amplifier that consists of two $4 \times 25\mu\text{m}$ offset gate HJFETs. The LNA was designed to have a higher gain rather than a lower N.F. to compensate for the conversion loss (14dB) of the mixer. The LNA was estimated to have an N.F. of 4.6dB and an associated gain of 12.8dB at 58GHz by measuring a 2-stage LNA test MMIC (Fig.4). The subharmonic mixer consists of a pair of anti-parallel $2 \times 12.5\mu\text{m}$ Schottky diodes, which have the same recess structure as the HJFETs, a $\lambda_{\text{RF}}/2$ short stub on the opposite side of the diode pair from the RF input, such that the diodes are terminated at the RF frequency, and a $\lambda_{\text{LO}}/4$ open stub on the opposite side of the diode pair from the LO input. The 30GHz local signal amplifier is a 2-stage resistive matched amplifier which was designed to have a 15dB gain and a 19dBm output power. Fig.5 shows the RF performance of the receiver chip. A conversion 2dB gain and a N.F. of 6.5dB have been measured with IF=500MHz and -3dBm local power. Fig.6 shows a microphotograph of this chip, whose size is only a mere 2.3mm x 0.84mm.

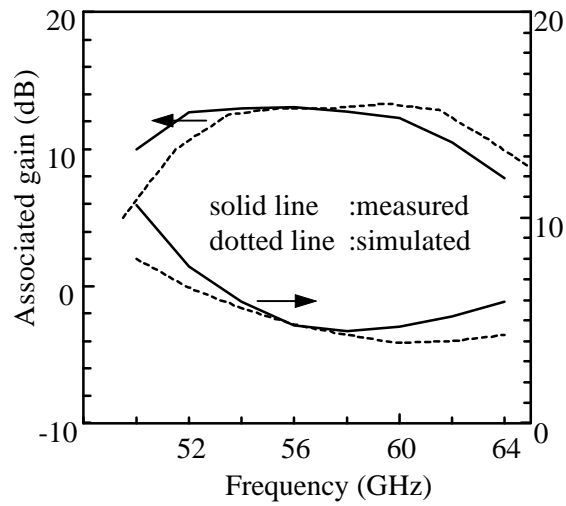


Fig.4 RF performance of 2-stage LNA

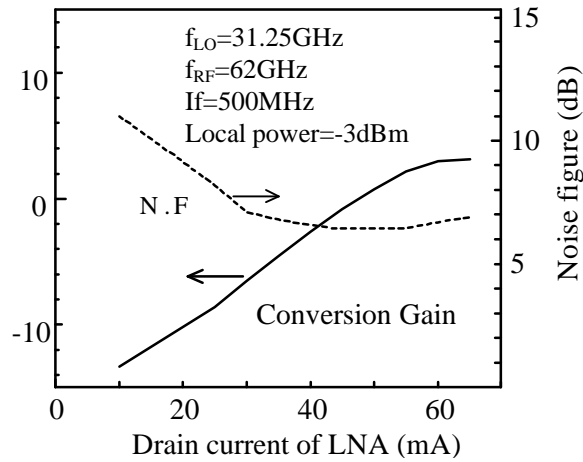


Fig.5 RF performance of receiver chip

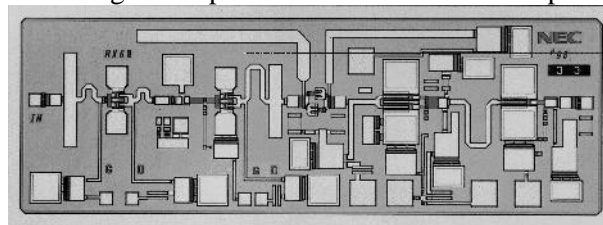


Fig.6 Receiver MMIC (2.3mm x 0.84mm)

V-band high performance transmitter MMIC

The V-band transmitter chip contains of a 30-60 GHz doubler and a 3-stage V-band amplifier (Fig.7). The doubler is composed of a $2 \times 100\mu\text{m}$ HJFET and a $\lambda/4$ open stub for a 30GHz output rejection and is connected to the amplifier at the conjugate condition of 60GHz. The doubler was designed to be unconditionally stable using an input series resistor, avoiding undesirable oscillation. The 3-stage amplifier consists of two $2 \times 100\mu\text{m}$ HJFETs and a single $4 \times 100\mu\text{m}$ HJFET. In order to realize broad-band performance as a transmitter MMIC as

opposed to the generally narrow-band characteristics of this type of doubler, the amplifier must have a broadband high gain. The 3-stage amplifier was estimated to have more than a 24dB gain from 48GHz to 61GHz by measuring a 3-stage amplifier test MMIC with the same structure (Fig.8). Fig.9 shows the RF performance of this transmitter MMIC. Maximum conversion gain of 14.3dB, and 17.7dBm output power at 56GHz and more than 15dBm power from 47.5GHz to 61GHz have been measured. Fig.10 shows a microphotograph of this chip which measures 2.3mm x 0.84mm.

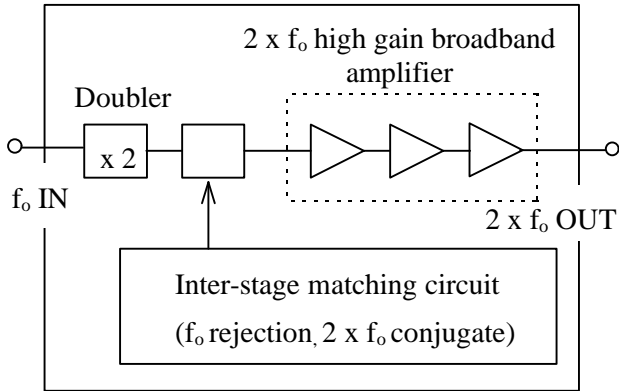


Fig.7 Block diagram of transmitter MMIC

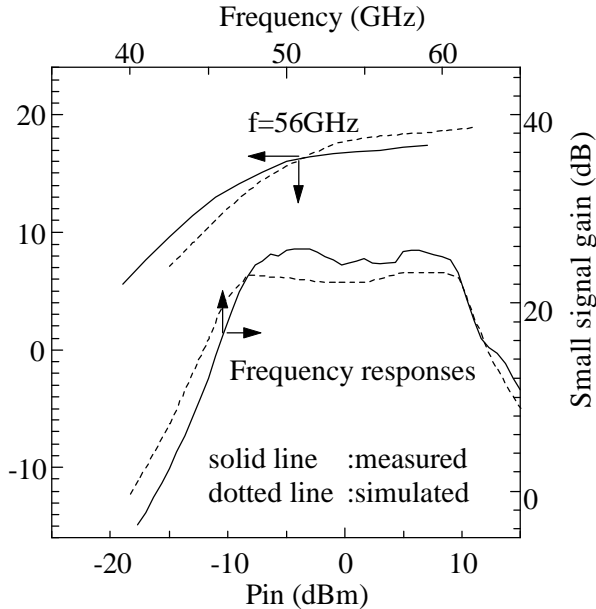


Fig.8 3-stage 60GHz amplifier

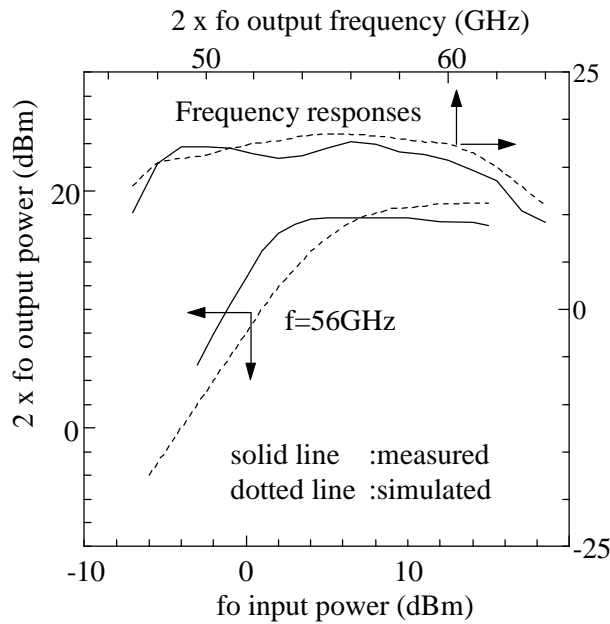


Fig.9 RF performance of 30-60GHz doubler

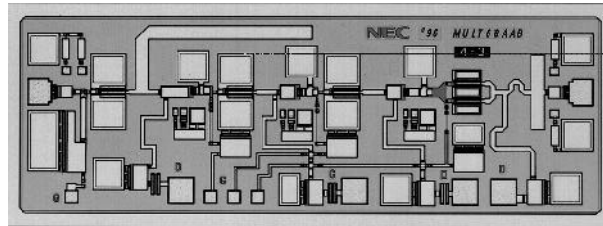


Fig.10 Microphotograph of doubler MMIC

Conclusion

A compact V-band transmitter/receiver MMIC chip set, consisting of a highly integrated receiver chip which exhibited good RF performance and a transmitter MMIC with state-of-the-art performance, has been successfully implemented with a highly reliable MMIC process such that the HJFETs of these MMICs exhibited an MTTF of 4×10^7 hours at T_{ch} of 130°C. These two MMICs can dramatically simplify some V-band RF systems since this system requires no V-band local signal and no power amplifiers.

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Reference

- [1] Y. Takimoto, "Recent Activities on Millimeter Wave Indoor LAN system Development in Japan," 1993 IEEE MTT-S Digest, pp.405-408.
- [2] M. Funahasi et.al., "High Gain V-Band Heterojunction FET MMIC Power Amplifier," 1993 IEEE GaAs IC Symp. Digest, pp 379- 382.
- [3] D.C.W.Lo, et.al., "A Single-Chip W-band Transceiver with Front-End Switching Receiver for FMCW Radar Applications", 1995 IEEE MTT-S, pp.873-876.

- [4] K. L.Tan et.al., "High-Power V-band Pseudomorphic InGaAs HEMT," IEEE Electron Device Lett.,vol.12, no.5, pp213-214,May 1991.
- [5] S. Raman et.al., "A 94GHz UNIPLANAR SUBHARMONIC MIXER," 1996 IEEE MTT-S Digest, pp 385-388.
- [6] H. Zireth, et.al., "A W-Band Subharmonically Pumped Resistive Mixer Based on Pseudomorphic Heterostructure Field Effect Transistor Technology," 1993 IEEE MTT-S Digest, Atlanta, GA, Jun. 14-18, 1993, pp.341-344.